Listing of Claims

1. (Currently Amended) A semiconductor device comprising:

a first conductivity type semiconductor region having a main surface;

an element isolation region isolating an active region;

second conductivity type source/drain regions formed on said main surface of said semiconductor region in the active region to hold a channel region therebetween at a prescribed interval;

a fluorine- or carbon-containing region extending from the element isolation region over a junction interface between said first conductivity type semiconductor region and said second conductivity type source/drain regions;

a gate electrode formed on said channel region through a gate insulator film; and

side wall insulator films formed on the side surfaces of said gate electrode~~, wherein fluorine has been introduced into at least one of the following: a region extending from the element isolation region over a junction interface between said first conductivity type semiconductor region and said second conductivity type source/drain regions; and said side wall insulator films~~.

2. (Currently Amended) The semiconductor device according to claim 1, wherein fluorine is ~~introduced into said regions extending over the junction interfaces between said first conductivity type semiconductor region and said second conductivity type source/drain regions,~~ present in at least the interface between the gate insulator film and the central region of said channel region as well as said gate insulator film, and said side wall insulator films.

3. (Original) The semiconductor device according to claim 1, wherein said first conductivity type semiconductor region includes a first conductivity type silicon region.

4. (Original) The semiconductor device according to claim 1, wherein said side wall insulator films consist of insulator films containing Si.

5. (Currently Amended) A semiconductor device comprising:

a first conductivity type semiconductor region having a main surface;

an element isolation region isolating an active region;

a second conductivity type impurity region formed on said main surface of said semiconductor region in the active region~~, wherein~~; and

~~an element of at least either~~ a fluorine- or carbon-containing ~~has been introduced into a~~ region extending from the element isolation region over a junction interface between said first conductivity type semiconductor region and said second conductivity type impurity region.

6. (Currently Amended) The semiconductor device according to claim 5, wherein said impurity region includes a low-concentration impurity region and a high-concentration impurity region, and

said ~~element of at least either~~ fluorine- or carbon-containing ~~has been introduced into at least a~~ region ~~extending~~ extends from the element isolation region over a junction interface between said first conductivity type semiconductor region and said high-concentration impurity region.

7. (Currently Amended) The semiconductor device according to claim 5, further comprising:

a gate electrode formed on said main surface of said semiconductor region through a gate insulator film, and

side wall insulator films formed on the side surfaces of said gate electrode, wherein

~~said element of at least either fluorine or carbon is introduced also into~~ said side wall insulator films contains either fluorine or carbon.

8. (Currently Amended) The semiconductor device according to claim 5, wherein

said impurity region includes second conductivity type source/drain regions formed on said main surface of said semiconductor region to hold a channel region therebetween at a prescribed interval,

said ~~element of at least either~~ fluorine- or carbon-containing region is a fluorine-containing region, and

~~said fluorine is introduced also into~~ at least the interface between the gate insulator film and the central region of said channel region as well as said gate insulator film contains fluorine.

Claims 9 - 17. (Cancelled)

18. (Withdrawn) A method of fabricating a semiconductor device, comprising steps of:

forming second conductivity type source/drain regions on the main surface of a first conductivity type semiconductor region to hold a channel region therebetween at a prescribed interval;

forming a gate electrode on said channel region through a gate insulator film;

forming side wall insulator films on the side surfaces of said gate electrode; and

introducing fluorine into at least any of regions extending over the junction interfaces between said first conductivity type semiconductor region and said second conductivity type source/drain regions, at least the interface between the gate insulator film and the central region of said channel region as well as said gate insulator film, and said side wall insulator films.

19. (Withdrawn) The method of fabricating a semiconductor device according to claim 18, wherein

said step of introducing fluorine includes a step of ion-implanting said fluorine into said gate electrode and thereafter performing heat treatment thereby diffusing said fluorine from said gate electrode into said side wall insulator films while diffusing said fluorine from said gate electrode into said gate insulator film and at least the interface between the gate insulator film and the central region of said channel region.

20. (Withdrawn) The method of fabricating a semiconductor device according to claim 18, wherein

said step of introducing fluorine includes a step of ion-implanting said fluorine into said regions extending over the junction interfaces between said first conductivity type semiconductor region and said second conductivity type source/drain regions.

21. (Withdrawn) A method of fabricating a semiconductor device, comprising steps of:

forming a second conductivity type impurity region on the main surface of a first conductivity type semiconductor region; and

introducing an element of at least either fluorine or carbon into a region extending over the junction interface between said second conductivity type impurity region and said first conductivity type semiconductor region.

22. (Withdrawn) The method of fabricating a semiconductor device according to claim 21, wherein

said step of forming said second conductivity type impurity region includes a step of forming a second conductivity type source/drain region including a low-concentration impurity region and a high-concentration impurity region, and

said step of introducing said element of at least either fluorine or carbon includes a step of introducing said element of at least either fluorine or carbon into at least a region extending over the junction interface between said first conductivity type semiconductor region and said high-concentration impurity region.

23. (Withdrawn) The method of fabricating a semiconductor device according to claim 21, wherein

said step of introducing said element of at least either fluorine or carbon includes a step of ion-implanting fluorine into said region extending over the junction interface between said

second conductivity type impurity region and said first conductivity type semiconductor region at an implantation dosage of at least about 1.5×10^{15} cm^{-2} and not more than about 3×10^{15} cm^{-2}.

24. (Withdrawn) A method of fabricating a semiconductor device, comprising steps of:

forming a gate electrode on the surface of a first conductivity type semiconductor region through a gate insulator film;

ion-implanting an element reducing the dielectric constant at least into said gate electrode;

forming side wall insulator films on the side surfaces of said gate electrode;

forming a silicon nitride film at least on said side wall insulator films; and

diffusing said element reducing the dielectric constant from said gate electrode into said side wall insulator films by heat treatment.

25. (Withdrawn) The method of fabricating a semiconductor device according to claim 24, wherein

said step of ion-implanting said element reducing the dielectric constant includes a step of implanting said element reducing the dielectric constant also into said first conductivity type semiconductor region, and

said step of diffusing said element reducing the dielectric constant from said gate electrode into said side wall insulator films includes a step of diffusing said element reducing the dielectric constant from said first conductivity type semiconductor region into said side wall insulator films by heat treatment.

26. (Withdrawn) A method of fabricating a semiconductor device, comprising steps of:

forming a gate electrode on the main surface of a silicon substrate through a gate insulator film;

ion-implanting a halogenic element into said gate electrode; and

diffusing said halogenic element in said gate electrode into said gate insulator film and the interface between said gate insulator film and said silicon substrate by heat-treating said silicon substrate.

27. (Withdrawn) The method of fabricating a semiconductor device according to claim 26, wherein

said halogenic element is fluorine.

28. (Withdrawn) The method of fabricating a semiconductor device according to claim 26, wherein

said step of ion-implanting said halogenic element includes a step of ion-implanting said fluorine at an implantation dosage of at least about 1.5×10^{15} cm^{-2} and not more than about 5×10^{15} cm^{-2}.

29. (Withdrawn) The method of fabricating a semiconductor device according to claim 26, wherein

said heat treatment for diffusing said halogenic element is performed only once after ion implantation of said halogenic element.

30. (Withdrawn) A method of fabricating a semiconductor device, comprising steps of:

forming a gate electrode on the main surface of a first conductivity type silicon substrate through a gate insulator film;

forming a pair of second conductivity type source/drain regions on the main surface of said silicon substrate to hold a channel region therebetween;

ion-implanting a halogenic element into said source/drain regions and said gate electrode; and

diffusing said halogenic element in said gate electrode into said gate insulator film and said channel region located on the interface between said gate insulator film and said silicon substrate while diffusing said halogenic element in said source/drain regions into said channel region located under said gate insulator film by heat-treating said silicon substrate.

31. (Currently Amended) A semiconductor device comprising:

a first conductivity type semiconductor region having a main surface;

an element isolation region isolating an active region;

second conductivity type source/drain regions formed on said main surface of said semiconductor region in the active region to hold a channel region therebetween at a prescribed interval;

a gate electrode formed on said channel region through a gate insulator film~~, and~~

side wall insulator films formed on the side surfaces of said gate electrode~~, wherein~~; and

~~fluorine is introduced into all of the following:~~ a fluorine-containing region extending from the element isolation region over a junction interface between said first conductivity type semiconductor region and said second conductivity type source/drain regions, wherein

at least the interface between the gate insulator film and the central region of said channel region as well as said gate insulator film, and said side wall insulator films contains fluorine.

Claims 32 - 35. (Cancelled)

36. (New) The semiconductor device according to claim 1, wherein

said fluorine- or carbon-containing region is provided on a region below said junction interface between said first conductivity type semiconductor region and said second conductivity type source/drain regions.

37. (New) The semiconductor device according to claim 5, wherein

said second conductivity type impurity region includes second conductivity type source/drain regions, and

said fluorine- or carbon-containing region is provided on a region below said junction interface between said first conductivity type semiconductor region and said second conductivity type source/drain regions.

38. (New) The semiconductor device according to claim 31, wherein

a fluorine- or carbon-containing region is provided on a region below said junction interface between said first conductivity type semiconductor region and said second conductivity type source/drain regions.